IN THE CLAIMS

Please amend Claims 1, 8 and 17-19 to read as follows. Also, please add a new independent Claim 20.

1. (Previously presented) A power consumption reduction circuit comprising:

a memory clock source of a graphics controller; and

a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.

2. (Original) The circuit of claim 1 further including an engine clock source operatively coupled to a switching circuit that generates an output clock signal that is selectively coupled as a clock signal to at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port such that the switching circuit disables the output clock signal based on at least one of the following condition data: standby mode data, video overlay enable data, video capture enable data, I2C enable data, and multimedia port enable data.

3. (Original) The circuit of claim 1 further including a variable memory clock control circuit operative to vary a speed of the memory clock based on a type of memory request from a plurality of memory requestors.

4. (Original) The circuit of claim 1 including a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

5. (Original) The circuit of claim 4 wherein the memory read latch control circuit generates a read latch enable signal and includes:

a read data latency compensation circuit; and

a gating circuit responsive to the read latch control signal and a memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests.

6. (Original) The circuit of claim 5 including a multiplexer having an output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output at least one of the memory clock signal or the memory clock feedback signal to emulate clock delay in the circuit layout.

7. (Previously presented) The circuit of claim 1 wherein the memory clock tree circuit includes a plurality of logic circuits, wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources

8. (Previously presented) A power consumption reduction circuit comprising:

a memory clock source of a graphics controller;

a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data;

an engine clock source operatively coupled to a switching circuit that generates an output engine clock signal that is selectively coupled as a clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port, such that the switching circuit disables the output engine clock signal in response to receiving condition data; and

a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

9. (Original) The circuit of claim 8 further including a variable memory clock control circuit operative to vary a speed of the memory clock based on a type of memory request from a plurality of memory requestors.

10. (Original) The circuit of claim 8 wherein the memory read latch control circuit generates a read latch enable signal and includes:

a read data latency compensation circuit; and

a gating circuit responsive to the read latch control signal and a memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests.

11. (Original) The circuit of claim 10 including a multiplexer having an output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output at least one of the memory clock signal or the memory clock feedback signal to emulate clock delay in the circuit layout.

12. (Previously presented) The circuit of claim 8 wherein the memory clock tree circuit includes a plurality of logic circuits, wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources.

13. (Previously presented) A power consumption reduction method comprising:

generating branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines;

selectively activating at least some of the plurality of independent clock signals in response to received condition data;

selectively coupling an engine clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port to selectively disable the output engine clock signal in response to receiving condition data; and

dynamically activating and de-activating a plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

14. (Original) The method of claim 13 further including varying a speed of the memory clock based on a type of memory request from a plurality of memory requestors.

15. (Original) The method of claim 13 including:

generating a read latch control signal based on a read data latency compensation duration; and

selectively enabling and disabling memory read latches based on the read latch control signal and as a function of memory requests.

16. (Original) The method of claim 13 including:

outputting one of the plurality of corresponding independent clock signals from a different divider circuit based on receiving different condition data associated with different condition data sources

17. (Previously presented) The circuit of Claim 1, wherein the received condition data includes data representing at least one of: whether a primary or secondary display has been selected, whether a graphic user interface engine is active, whether a video overlay scaler has been enabled, whether subpicture operation has been enabled, and whether video capture operations have been enabled.

18. (Previously presented) The circuit of Claim 8, wherein the received condition data includes data representing at least one of: whether a primary or secondary display has been selected, whether a graphic user interface engine is active, whether a video overlay scaler has been enabled, whether subpicture operation has been enabled, and whether video capture operations have been enabled.

19. (Previously presented) The method of Claim 13, wherein the received condition data includes data representing at least one of: whether a primary or secondary display has been selected, whether a graphic user interface engine is active, whether a video overlay scaler has been enabled, whether subpicture operation has been enabled, and whether video capture operations have been enabled.

20. (New) A power consumption reduction circuit comprising:

a memory clock source of a graphics controller; and

a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of

corresponding independent clock signals to a number of memory interface circuits for differing processing engines without re-ordering instructions generated by a source code compiler if a source code compiler is in the graphics controller, and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.